North-Holland
Microprocessing and Microprogramming 30 (1990) 715-718



# Subject Index


Addressing processor 30 (1990) 657
ASICS 30 (1990) 263
Automation of models generation 30 (1990) 223

Backward error recovery 30 (1990) 371
Behavioral circuit description 30 (1990) 561
Broadcast network 30 (1990) 637
Bus-monitor unit 30 (1990) 521

Cache memories 30 (1990) 135
Cache simulator 30 (1990) 135
CCM algorithm 30 (1990) 51
Cellular architecture 30 (1990) 249
CISC 30 (1990) 21
CISC processor 30 (1990) 665
CMOS layout generation 30 (1990) 509
CMOS technology 30 (1990) 33
Co-programming software design style 30 (1990) 569
Code generation 30 (1990) 475
Code optimization 30 (1990) 475
Coherence protocol 30 (1990) 207
COIN model 30 (1990) 569
Communication kernel 30 (1990) 703
Compiler hardware structures 30 (1990) 555
Computer structures 30 (1990) 555
Contiguous / sparsed vectors 30 (1990) 657
Controller synthesis 30 (1990) 313
Controlpath synthesis 30 (1990) 117
CORDIC algorithm 30 (1990) 51
Correlation coefficients 30 (1990) 609
Current computation 30 (1990) 577

Data acquisition with on-line processing 30 (1990) 67
Data flow 30 (1990) 585,601
Data flow diagrams 30 (1990) 357
Data parallelism 30 (1990) 77
Data types 30 (1990) 555
Deadlock 30 (1990) 695,703
DES-algorithm 30 (1990) 59
Design-trajectory 30 (1990) 177
Digital circuits 30 (1990) 539
Distributed databases 30 (1990) 637
Distributed simulation 30 (1990) 215
DSP processor 30 (1990) 51
Dynamic load balancing 30 (1990) 77

Encryption 30 (1990) 59
Error detection mechanisms 30 (1990) 513
Event processing 30 (1990) 167

Fault injection experiments 30 (1990) 513
Fault simulator 30 (1990) 413,529
Fault tolerance 30 (1990) 9,371,617
Fault-tolerant system configurations 30 (1990) 521
Formal specification 30 (1990) 381
Formal specification/verification 30 (1990) 539
Function computation with polynomial expansion 30 (1990) 67

Gather/scatter 30 (1990) 657
Gaussian elimination 30 (1990) 153
Geometric parallelism 30 (1990) 77

Hard real-time systems 30 (1990) 389
Hardware correctness 30 (1990) 421
Hardware description languages 30 (1990) 223
Hardware design 30 (1990) 555
Hardware/software system design 30 (1990) 545
High level synthesis 30 (1990) 103

Image processing 30 (1990) 333
Image processing algorithms 30 (1990) 447
Image template matching 30 (1990) 609
Imperative programs 30 (1990) 185
Implementation technique 30 (1990) 397
Implementation testing 30 (1990) 297
Improved testability 30 (1990) 509
Integrated circuits design 30 (1990) 555
Interactive design and simulation system 30 (1990) 241
Interactive Space-Time Scheduler 30 (1990) 109
Interprocess communication synthesis 30 (1990) 695
IRCAM signal processing workstation 30 (1990) 167

Joint optimization 30 (1990) 637

KEDS protocol 30 (1990) 627

Layout compaction 30 (1990) 231
Logic programming techniques 30 (1990) 193
Logic synthesis 30 (1990) 313

Massively parallel architecture 30 (1990) 33
Massively parallel computer simulation 30 (1990) 569
Massively parallel computers 30 (1990) 569
Mathematician's Devil 30 (1990) 593
Message passing 30 (1990) 645
Metropolitan Area Network 30 (1990) 627
Microprogrammed applications 30 (1990) 67
Modular neural network architecture 30 (1990) 257
Molecular dynamics 30 (1990) 159
Multiprocessor machine 30 (1990) 601

Neighbour searching 30 (1990) 159
Neural net emulation 30 (1990) 249
Nuclear electronics 30 (1990) 67
Number format converter 30 (1990) 237

Object-oriented communication 30 (1990) 569
Object-oriented compiler target language 30 (1990) 457
Occam 30 (1990) 85,93
Operative part 30 (1990) 555
Optimizing transformations 30 (1990) 185
OTTER 30 (1990) 421

Parallel architecture 30 (1990) 215,439,609
Parallel architecture compiler 30 (1990) 467
Parallel computing systems 30 (1990) 585
Parallel execution 30 (1990) 103
Parallel Inference Machine 30 (1990) 201
Parallel languages 30 (1990) 569
Parallel programming 30 (1990) 365
Partitioned algorithms 30 (1990) 153
Partitioning 30 (1990) 609
PASCAL 30 (1990) 365
PASS 30 (1990) 103
Path-disjoint routing 30 (1990) 93
Performance analysis 30 (1990) 601,683
Petri Nets 30 (1990) 193,389

Pipelining 30 (1990) 665
Program development 30 (1990) 593
Pyramidal architecture 30 (1990) 569

Quasi dynamic approach 30 (1990) 231

Rational methodology 30 (1990) 555
Real Time software 30 (1990) 357
Real-time distributed systems 30 (1990) 499
Real-time functional programming systems 30 (1990) 491
Real-time multi-channel protocols 30 (1990) 485
Real-time processing 30 (1990) 167
Real-time system 30 (1990) 9,381,397
Real-time video coding 30 (1990) 439
Reconfigurable processor arrays 30 (1990) 153
Recovery meta program 30 (1990) 371
Register file 30 (1990) 143
Requirements analysis 30 (1990) 289
Requirements capture and analysis 30 (1990) 281
Responsive systems 30 (1990) 9
Reverse engineering 30 (1990) 357
RISC-architecture 30 (1990) 21,33,41,127

Scan conversion 30 (1990) 431
Sequential machines 30 (1990) 305
Simulated annealing 30 (1990) 85
Simulation acceleration 30 (1990) 233
Simulation of digital circuits 30 (1990) 223
Simultaneous decomposition 30 (1990) 305
Singly-buffered channels 30 (1990) 645
Software engineering 30 (1990) 357
Software library 30 (1990) 333
Software maintenance 30 (1990) 357
Software production 30 (1990) 273
Software-hardware migration 30 (1990) 263
Solids 30 (1990) 341
Specification testing 30 (1990) 297
Static algorithms 30 (1990) 109
Stepwise decomposition 30 (1990) 117
Supercomputer 30 (1990) 657
System level language 30 (1990) 561
Systolic array 30 (1990) 609
Temporal agent model 30 (1990) 499

Test pattern sets 30 (1990) 413
Testability 30 (1990) 405
Tightly coupled multiprocessor systems 30 (1990) 207
Timed Petri Nets implementation 30 (1990) 313
Toriodal mesh networks 30 (1990) 683
Transputer 30 (1990) 77,85,93,159,347,529

User-oriented models 30 (1990) 289

Vector addressing 30 (1990) 657
Vector memory 30 (1990) 657
Vector processing 30 (1990) 657
VLSI design 30 (1990) 321
VLSI design tools 30 (1990) 223
VOXEL 30 (1990) 341
VUXAR project 30 (1990) 347

North-Holland
Microprocessing and Microprogramming 30 (1990) 719-724



## Author Index

Accomazzo, E., Ancona, M., Bobbio, R., Cagnassi, C., and Paolin, L., Integrating intermediate code optimization with retargetable code generation 30 (1990) 475
Ahn, J.K., and Moon S.C., Join optimization in distributed databases on broadcast network 30 (1990) 637
Ancona, M., see Accomazzo, E. 30 (1990) 475
Andre, C., and Fancelli, L., A mixed implementation of a real-time system 30 (1990) 397
Annaiyappa, P.K., see Karshmer, A.I. 30 (1990) 21
Antoniazzi, S., and Mastretti, M., An interactive environment for hardware/software system design at the specification level 30 (1990) 545
Argüello, F., see Zapata, E.L. 30 (1990) 609
Arkko, J., Hirvisalo, V., Kuusela, J., and Nuutila, E., Supporting testing of specifications and implementations 30 (1990) 297
Arregi, O., Rodríquez, C., and Ibarra, A., Evaluation of the optimal strategy for managing the register file 30 (1990) 143
Assuncão, P., see Sá, L. de 30 (1990) 439
Auer, A., Levanto, M., Okkonen, A., and Okkonen, J., Solution in software crisis 30 (1990) 273
Auguin, M., Boeri, F., Carriere, C., and Menez, G., From progam to hardware: a parallel architecture compiler 30 (1990) 467
Austin, J., see Macharia, G.M. 30 (1990) 657

Bakowski, P., see Dubois, J.-L. 30 (1990) 223
Balakrishnan, S., and Nandy, S.K., Quasi dynamic approach to layout compaction 30 (1990) 231
Balou, A.T., and Refenes, A.N., Designing a parallel object-oriented compiler target language (TOOL) 30 (1990) 457
Bandyopadhayay, A.K., see Pramanik, P. 30 (1990) 703
Barbosa, F.M.B., see Vasconcelos, N.Q. 30 (1990) 365
Barbosa V.C., and Boeres M.C.S., An Occam-based evaluation of a parallel version of simulated annealing 30 (1990) 85
Bechennec, J-L., see Cappello, F. 30 (1990) 41
Beck, M., see Tavangarian, D. 30 (1990) 41
Bekker, H., and Renardus, M., Design of a transputer network for searching neighbours in M.D. simulations 30 (1990) 159
Beller, W., see Kropf, T. 30 (1990) 59
Beltman, A.J., see Spaanenburg, L. 30 (1990) 263
Benson, T.J.G., Milligan, P., and Scott, N.S., Program development within the Mathematician's Devil 30 (1990) 593
Berbers, Y., see Joosen, W. 30 (1990) 77
Bobbio, M., see Accomazzo, E. 30 (1990) 475
Boeres, M.C.S., see Barbosa V.C. 30 (1990) 85
Boeri, F., see Auguin, M. 30 (1990) 467
Bormans J.E.H.M., Withagen, W.J., Budzelaar, F.P.M., and Stevens M.P.J., Designing high performance instruction caches in VLSI 30 (1990) 135
Bouaziz, S., see Pissaloux, E.E. 30 (1990) 569
Bragagnini, W., Guazzoni, P., Pitalieri, M., and Zetta, L., Computational logic unit for a microprogrammed data acquisition system: an evaluation prototype 30 (1990) 67
Budzelaar, F.P.M., see Bormans, J.E.H.M. 30 (1990) 135
Budzelaar, F.P.M., see Stevens, M.P.J. 30 (1990) 321
Buhler, P., The COIN model for concurrent computation and its implementation 30 (1990) 577
Buonanno, G., Burri, A., Fummi, F., and Sciuto, D., An approach to a design for testability personal consultant 30 (1990) 405
Burri, A., see Buonanno, G. 30 (1990) 405

Cabaleiro, J.C., see Zapata, E.L. 30 (1990) 609
Cabodi, G., Gai, S., and Sonza Reorda, M., A transputer-based gate-level fault simulator 30 (1990) 529
Cagnassi, C., see Accomazzo, E. 30 (1990) 475
Camurati, P., Lioy, A., Prinetto, P., and Sonza Reorda, M., Assessing the diagnositic power of test pattern sets 30 (1990) 413
Camurati, P., Margaria, T., and Prinetto, P., The OTTER environment for resolution-based proof of hardware correctness 30 (1990) 421
Canfora, G., Cimitile, A., and De Carlini, U., Reverse engineering and data flow diagrams in ADA environment 30 (1990) 357
Cappello, F., Bechennec, J-L., and Etiemble, D., A RISC central processsing unit for a massivelly parallel architecture 30 (1990) 41
Carpenter, G.F., see Tyrrell, A.M. 30 (1990) 585
Carpenter, G.F., The synthesis of deadlock-free interprocess communications 30 (1990) 695
Carracieri, G., see Maresca, M. 30 (1990) 153
Carriere, C., see Auguin, M. 30 (1990) 467
Caubet, R., see Pitot, P. 30 (1990) 347
Cimitile, A., see Canfora, G. 30 (1990) 357
Clematis, A., Dodero, G. and Gianuzzi, V., Recovery Meta Program in Unix based environment 30 (1990) 371
Concalo, Q., see Madeira, H. 30 (1990) 513
Cooling, J.E., see Huges, T.S. 30 (1990) 381

Das, P.K., see Pramanik, P. 30 (1990) 703
De Carlini, U., see Canfora, G. 30 (1990) 357
Dekeyser, J-L., Marquet, P., and Preux, P., Vector addressing processor for direct and indirect accesses 30 (1990) 657
Devos, A., see Pissaloux, E.E. 30 (1990) 569
Dimitriadis, B., see Parthenis, K. 30 (1990) 333
Dirkx, E., Verboven, F., and Tiberghien, J., Distributed simulation of computer networks 30 (1990) 215
Doallo, R., see Zapata, E.L. 30 (1990) 609
Dodero, G., see Clematis, A. 30 (1990) 371
Domenici, A., Petri nets in logic 30 (1990) 193
Dubois, J.-L., Bakowksi, P., and Pawlak, A., Synthesis of programmable control structures for a simulation speed-up 30 (1990) 223
Duthen, Y., see Pitot, P. 30 (1990) 347

Eshner, D., see Karshmer, A.I. 30 (1990) 21
Etiemble, D., see Cappello, F. 30 (1990) 41
Ewering, C., and Gerhardt, G., PASS: high level synthesis 30 (1990) 103

Fancelli, L., see Andre, C. 30 (1990) 397
Faria, S., see Sá, L. de 30 (1990) 439
Faure, B., and Mazare, G., A cellular architecture dedicated to neural net emualation 30 (1990) 249
Fay, D.Q.M., see Pramanik, P. 30 (1990) 703
Fernandes, E.S.T., see Vasconcelos, N.Q. 30 (1990) 365
Franken, P.B., and A.J. van de Goor, Special architecture for high-performance scan conversion 30 (1990) 431
Frisiani, A.L., see Maresca, M. 30 (1990) 153
Frösse, J., see Kropf, T. 30 (1990) 59
Fummi, F., see Buonnano, G. 30 (1990) 405

Gai, S., see Cabodi, G. 30 (1990) 529
Gajda, R., Thor, M., and Tudruj, M., Enhancing a control graph based HDL for performance evaluation of simulated architectures 30 (1990) 683
Geidemen, W.A., Niederland, R.A., and Harrington, D.A., A 32-bit RISC CPU implemented in GaAs 30 (1990) 127
Geisler, T., see Kropf, T. 30 (1990) 59
Gerardt, G., see Ewering, C. 30 (1990) 103
Gianuzzi, V., see Clematis, A. 30 (1990) 371
Glass, D., see McChesney, I. 30 (1990) 281

Goor, A.J. van de, see Franken, P.B. 30 (1990) 431
Gornara, G., see Maresca, M. 30 (1990) 153
Goutis, C.E., see Matafas, D.E. 30 (1990) 51
Goutis, C.E., see Kyrologlou, N.A. 30 (1990) 237
Graaff, P.J. de, On the formal specification and verification of digital circuits 30 (1990) 539
Guazzoni, P., see Bragagnini, W. 30 (1990) 67

Harrington, R.A., see Geideman, W.A. 30 (1990) 127
Hirvisalo, V., see Arkko, J. 30 (1990) 297
Hoekstra, J., System architecture of a modular neural network using 400 simple processors 30 (1990) 249
Holding, D.J., see Sagoo, J.S. 30 (1990) 389
Hong Shen, Occam implementation of path-disjoint routing on the Hathi-2 transputer system 30 (1990) 93
Huang, S., see Xu, J. 30 (1990) 617
Hughes, T.S. and Cooling, J.E., Animation prototyping of formal specifications of real-time systems 30 (1990) 381
Hughes, J.G., see McChesney, I. 30 (1990) 281
Huis in 't Veld, R.J., The role of languages in the design-trajectory 30 (1990) 177

Ibbara, A., see Arregi, O. 30 (1990) 143

Jokela, T., and Lindberg, K., Statecharts based requirements analysis: deriving user oriented models 30 (1990) 289
Joosen, W., Berbers, Y., and Verbaeten, P., Dynamic load balancing in transputer applications with geometric parallelism 30 (1990) 77
Jóźwiak, L., Simultaneous decompositions of sequential machines 30 (1990) 305

Kankanahalli, S., see Karshmer, A.I. 30 (1990) 21
Kanopoulos, N., see Markas, T. 30 (1990) 521
Kapus-Kolar, M., Constructing real-time multi-channel protocols 30 (1990) 485
Karshmer A.I., Thomas, J.N., Annaiyappa, P.K., Eshner, D., Kankanahalli, S., and Kurup G., Architectural support of operating systems: a popular RISC vs a popular CISC 30 (1990) 21
Karshmer, A.I., and Thomas J.N., TVNet II: a cable TV based metropolitan area network using the KEDS protocol 30 (1990) 627
Kock, G., Towards the verification of optimizing transformations for imperative programs 30 (1990) 185
Koufopavlou, G., see Kyrologlou, N.A. 30 (1990) 237
Kropf, T., Frösse, J., Beller W., and Giesler, T., A hardware implementation of a modified DES-algorithm 30 (1990) 59
Kurup, G., see Karshmer, A.I. 30 (1990) 21
Kuusela, J., see Arkko, J. 30 (1990) 297
Kyrloglou, N.A., Koufopavlou, G., and Goutis, C.E., A generator for a number format conversion IC 30 (1990) 237

Levanto, M., see Auer, A. 30 (1990) 273
Lindberg, K., see Jokela, T. 30 (1990) 289
Lindemann, E., Puckette, M., Viara, E., and Starkier, M., The IRCAM signal processing workstation - an environment for research in real-time signal processing and performance 30 (1990) 167
Lioy, A., see Camurati, P. 30 (1990) 413
Lisper, B., The interactive space-time scheduler 30 (1990) 109

Macharia, G.M., and Austin, J., A performance analysis of toroidal mesh networks 30 (1990) 675
Madeira, H., Concalo, Q., and Silva, J.G., Experimental evaluation of a set of simple error detection mechanisms 30 (1990) 513
Malek, M., Responsive systems: a challenge for the nineties 30 (1990) 9

Maresca, M., Carracieri, G., Cornara, G., and Frisiani, A.L., Partitioned algorithms for Gaussian elimination on reconfigurable processor arrays 30 (1990) 153
Margaria, T., see Camurati, P. 30 (1990) 421
Markas, T., and Kanopoulos, N., A bus-monitor unit for fault-tolerant system configurations 30 (1990) 521
Marquet, P., see Dekeyser, J-L. 30 (1990) 657
Mastretti, M., see Antoniazzi, S. 30 (1990) 545
Matafas, D.E., and Goutis, C.E., A DSP processor with a powerful set of elementary arithmetic operations based on CORDIC and CCM algorithms 30 (1990) 51
Mazare, G., see Faure, B. 30 (1990) 249
McChesney, I., Glass, D., and Hughes, J.G., Case tool support for requirements capture and analysis 30 (1990) 281
Menez, G., see Auguin, M. 30 (1990) 467
Mérigot, A., see Pissaloux, E.E. 30 (1990) 569
Metaxaki-Kossionidis, C., see Parthenis, K. 30 (1990) 333
Milligan, P., see Benson, T.J.G. 30 (1990) 593
Moisan, B., see Pitot, P. 30 (1990) 347
Moon, S.C., see Ahn, J.K. 30 (1990) 637

Nandy, S.K., see Balakrisnan, S. 30 (1990) 231
Nandy, S.K., see Prakash, C.E. 30 (1990) 341
Narayan, R., and Rajaraman, V., Performance analysis of a multiprocessor machine based on data flow principles 30 (1990) 601
Neale, D.F., see Winter, S.C. 30 (1990) 491
Niederland, R.A., see Geideman, W.A. 30 (1990) 127
Nijhuis, J.A.G., see Spaanenburg, L. 30 (1990) 263
Nuutila, E., see Arkko, J. 30 (1990) 297

Okkonen, J., see Auer, A. 30 (1990) 273
Okkonen, A., see Auer, A. 30 (1990) 273

Paolin, L., see Accomazzo, E. 30 (1990) 475
Parthenis, K., Metaxaki-Kossionidis, C., and Dimitriadis, B., EIKON: A software library for image processing applications 30 (1990) 333
Patel, M.R.K., Random logic circuit implementation of extended timed Petri nets 30 (1990) 313
Pawlak, A., see Dubois, J.-L. 30 (1990) 223
Perdigão, F., see Sá, L. de 30 (1990) 439
Pissaloux, E.E., Bouaziz, S., Mérigot, A., and Devos, A., Co-programmng : a tool for the development of software for massively parallel computers 30 (1990) 569
Pissaloux, E.E., A rational methodology for design of new computer structures 30 (1990) 555
Pitalieri, M., see Bragagnini, W. 30 (1990) 67
Pitot, P., Moisan, B., Duthen, Y., and Caubet, R., A transputer based implementation of the VOXAR project 30 (1990) 347
Pombortis, A., see Vlahavas, J. 30 (1990) 201
Prakash, C.E., and Nandy, S.K., VOXEL based modeling and rendering irregular solids 30 (1990) 341
Pramanik, P., Das, P.K., Bandyopadhyay, A.K. and Fay, D.Q.M., A deadlock-free communication kernel for loop connected message passing computer architecture 30 (1990) 703
Prete, C.A., A new solution of coherence protocol for tightly coupled multiprocessor systems 30 (1990) 207
Preux, P., see Dekeyser, J-L. 30 (1990) 657
Prinetto, P., see Camurati, P. 30 (1990) 421
Prinetto, P., see Camurati, P. 30 (1990) 413
Puckette, M., see Lindemann, E. 30 (1990) 167

Rajaraman, V., see Narayan, R. 30 (1990) 601
Refenes, A.N., Message passing via singly-buffered channels: an efficient and flexible communications control mechanism 30 (1990) 645
Refenes, A.N., see Balou, A.T. 30 (1990) 457

Reitsma, A., see Spaanenburg, L. 30 (1990) 263
Renardus, M., see Bekker, H. 30 (1990) 159
Rodriquez, O., see Arregi, O. 30 (1990) 143

Sá, L. de, Silva, V., Perdigão, F., Faria, S., and Assuncão, P., A parallel architecture for real-time video coding 30 (1990) 439
Sagoo, J.S., and Holding, D.J., The specification and design of hard real-time systems using timed and temporal Petri nets 30 (1990) 389
Scholefield, D., and Zedan, H., TAM: Temporal Agent Model for real-time distributed systems 30 (1990) 499
Sciuto, D., see Buonanno, G. 30 (1990) 405
Scott, N.S., see Benson, T.J.G. 30 (1990) 593
Silva, J.G., see Madeira, H. 30 (1990) 513
Silva, V., see Sá, L. de 30 (1990) 439
Smeets, J.P.C.F.H., Withagen, W.J., and Stevens M.P.J., Pipelining a memory based CISC processor 30 (1990) 665
Sonza Reorda, M., see Camurati, P. 30 (1990) 413
Sonza Reorda, M., see Cabodi, G. 30 (1990) 529
Spaanenburg, L., Beltman, A.J., Nijhuis, J.A.G., and Reitsma, A., A case study in the migration of software to hardware using ASICS 30 (1990) 263
Stamatis, D., see Vlahavas, J. 30 (1990) 201
Starkier, M., see Lindemann, E. 30 (1990) 167
Stern, O., and Vierhaus, H.T., CMOS layout generation for improved testability 30 (1990) 509
Stevens, M.P.J., and Budzelaar, F.P.M., System level VLSI design 30 (1990) 321
Stevens, M.P.J., see Smeets, J.P.C.F.H. 30 (1990) 665
Stevens, M.P.J., see Bormans, J.E.H.M. 30 (1990) 135

Tavangarian, D., and Beck, M., ASTRA: an associative RISC-architecure 30 (1990) 41
ten Berg, A.J.W.M., Stepwise decomposition in controlpath synthesis 30 (1990) 117
Thomas, J.N., see Karshmer, A.I. 30 (1990) 627
Thomas, J.N., see Karshmer, A.I. 30 (1990) 21
Thor, M., see Gajda, R. 30 (1990) 683
Tiberghien, J., see Dirkx, E. 30 (1990) 215
Tudruj, M., see Gajda, R. 30 (1990) 683
Tyrrell, A.M., and Carpenter, G.F., Data flow methods in the design of parallel computing systems 30 (1990) 585

Vajda, F., Application and implementation of window-based image processing algorithms 30 (1990) 447
Vasconcelos, N.Q., Fernandes, E.S.T., and Barbosa, F.M.B., An environment for parallel programming in PASCAL 30 (1990) 365
Verbaeten, P., see Joosen, W. 30 (1990) 77
Verboven, F., see Dirkx, E. 30 (1990) 215
Verschueren, A.C., An object oriented design and simulation system for VLSI 30 (1990) 241
Viara, E., see Lindemann, E. 30 (1990) 167
Vierhaus, H.T., see Stern, O. 30 (1990) 509
Vlahavas, J., Pombortsis, A., and Stamatis, D., Towards a parallel inference machine: the APIM project 30 (1990) 201

Wienkop, U., Behavioral circuit description on system level 30 (1990) 561
Wilson, D.R., see Winter, S.C. 30 (1990) 491
Winter, S.C., Wilson, D.R., and Neale, D.F., Real-time functional programming systems 30 (1990) 491
Withagen, W.J., see Smeets, J.P.C.F.H. 30 (1990) 665
Withagen, W.J., see Bormans, J.E.H.M. 30 (1990) 135

Xu, J., and Huang S., A new comparison-based scheme for multiprocessor fault tolerance 30 (1990) 617

Zapata, E.L., Cabaleiro, J.C., Doallo, R., and Argüello, F., Systolic architecture for the calculation of the correlation coefficients 30 (1990) 609
Zedan, H., see Scholefield, D. 30 (1990) 499
Zetta, L., see Bragagnini, W. 30 (1990) 67